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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/601,038	06/19/2003	Xuewen Jiang	42P15897	8243

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EXAMINER	
NGUYEN, LINH V	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 10/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

AA

Office Action Summary	Application No.	Applicant(s)	
	10/601,038	JIANG ET AL.	
	Examiner	Art Unit	
	Linh V Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-15,17- 20* is/are rejected.

7)☒ Claim(s) *6,16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application No. 10/601,038 filed on 06/19/03. Claims 1 – 20 are pending on this application.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 – 5, and 7 - 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Valdenaire U.S. Patent No. 5,455,582.

Regarding claim 1, Fig. 5 of Valdenaire disclose an apparatus comprising: a first segment (10 – 12) comprising a first (10a – 12a [R 2R ladder]) and second (10b – 12b [R 2R ladder]) ladders and having a differential input (10a, 10b); a second segment (13 [2R 2R ladder]) coupled to said first segment and having a differential output (14 Vp, 15 Vn); and at least one or more switches (S1, S2, S3) coupled between said first and

second ladders to switch between said first (10a – 12a [R 2R ladder]) and second (10b – 12b [R 2R ladder]) ladders ; wherein a differential digital signal (Vrefp, Vrefn) received at the differential input is converted to a differential analog signal at the differential output (Col. 2 lines 58 – 63, Also See Fig 7B [72]).

Regarding claim 4, wherein the first (10a – 12a [R 2R ladder]) and second (10b – 12b [R 2R ladder]) ladders comprise R2R ladders.

Regarding claim 5, wherein said second segment (13 section, [2R 2R ladder]) comprises a 2R pair array.

Regarding claim 7, Fig. 4 of Valdenaire further comprising an impedance element (R element between node 12a and S3+; and R element between node 12b and S3-) to couple said first segment (10 – 12 [R 2R ladder]) and said second segment (13 [2R 2R ladder]).

Regarding claim 8, wherein the first (10a – 12a [R 2R ladder]) and second (10b – 12b [R 2R ladder]) ladders comprise R2R ladders and said second segment (13b [2R 2R]) comprises a 2R pair array, said apparatus further comprising a resistor (R element between node 12a and S3+; and R element between node 12b and S3-) having a nominal value of R to couple said first segment (10 - 12 [R 2R ladder]) and said second segment (13 [2R 2R]).

Regarding claim 9, wherein the first (10a – 12a [R 2R ladder]) and second (10b – 12b [R 2R ladder]) ladders comprise R2R ladders and said second segment (13b [2R 2R]) comprises a 2R pair array, and wherein resistors of the first ladder are cross mixed with the second ladder resistors (Fig. 5 disclosing first [10a – 12a] and second [10b –

12b] R2R ladders are cross mixed through the switches) on an integrated circuit (Col. 1 lines 13 – 14).

Regarding claim 10, Fig. 7 of Valdenaire further comprising a filter (R3, R2, C1, C2 filter circuit, See Col. 8 lines 4 – 23) coupled to the differential output (Vp, Vn), wherein said filter has a gain sufficient to not require a buffer between the differential output and the filter (Fig. 7 does not disclose any buffer located between the Filter and the differential output Vp, Vn of R- 2R Digital to Analog converter 72, therefore the filter of Valdenaire must has a sufficient gain).

Regarding claim 2, wherein said first segment is a least significant bit section (Fig. 5 of Valdenaire as applied to claim 1 above and on Col. 3 lines 5 - 9, disclosing first segment 10 – 12 [R 2R] having differential input [10a and 10b] is a most significant bit section and second segment 13 [2R 2R] couple to the first segment having differential output [15 Vp, 14 Vn] is a least significant bit section). Furthermore, on Col.7 lines 32 – 34, Valdenaire teaches the node [14, 15] is a reference input, and the differential input [10a, 10b] is an output node. Hence 14 and 15 become the input nodes, and 10a and 10b become the output nodes in Fig. 5., the segment (13 [2R 2R]) now having differential input (14, 15), the segment (10 – 12 [R 2R]) now having differential output [10a 10b], wherein the segment (13 [2R 2R]) is a least significant bit section and the segment (10 – 12[R 2R]) is a most significant bit section (Col. 3 lines 5 – 9).

Regarding claim 3, wherein said second segment is a most significant bit section (Fig. 5 of Valdenaire as applied to claim 1 above and on Col. 3 lines 5 - 9, disclosing

first segment 10 – 12 [R 2R] having differential input [10a and 10b] is a most significant bit section and second segment 13 [2R 2R] couple to the first segment having differential output [15 Vp, 14 Vn] is a least significant bit section). Furthermore, on Col.7 lines 32 – 34, Valdenaire teaches the node [14, 15] is a reference input, and the differential input [10a, 10b] is an output node. Hence 14 and 15 become the input nodes, and 10a and 10b become the output nodes in Fig. 5., the segment (13 [2R 2R]) now having differential input (14, 15), the segment (10 – 12 [R 2R]) now having differential output [10a 10b], wherein the segment (13 [2R 2R]) is a least significant bit section and the segment (10 – 12[R 2R]) is a most significant bit section (Col. 3 lines 5 – 9).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 11 – 15, and 17 - 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Valdenaire as applied above, in further view of Dogan U.S Patent No. 6,650,881.

Regarding claim 11, Fig. 5 of Valdenaire discloses a digital to analog converter (Col. 1 lines 13 – 14), comprising: a first segment (10 – 12) comprising a first (10a – 12a

[R 2R ladder]) and second (10b – 12b [R 2R ladder]) ladders and having a differential input (10a, 10b); a second segment (13 [2R 2R ladder]) coupled to said first segment and having a differential output (14 Vp, 15 Vn); and at least one or more switches (S1, S2, S3) coupled between said first and second ladders to switch between said first (10a – 12a [R 2R ladder])) and second (10b – 12b [R 2R ladder]) ladders ; wherein a differential digital signal (Vrefp, Vrefn) received at the differential input is converted to a differential analog signal at the differential output (Col. 2 lines 58 – 63, Also See Fig 7B [72]).

Regarding claim 14, wherein the first (10a – 12a [R 2R ladder]) and second (10b – 12b [R 2R ladder]) ladders comprise R2R ladders.

Regarding claim 15, wherein said second segment (13 section, [2R 2R ladder]) comprises a 2R pair array.

Regarding claim 17, Fig. 4 of Valdenaire further comprising an impedance element (R element between node 12a and S3+; and R element between node 12b and S3-) to couple said first segment (10 – 12 [R 2R ladder]) and said second segment (13 [2R 2R ladder]).

Regarding claim 18, wherein the first (10a – 12a [R 2R ladder]) and second (10b – 12b [R 2R ladder]) ladders comprise R2R ladders and said second segment (13b [2R 2R]) comprises a 2R pair array, said apparatus further comprising a resistor (R element between node 12a and S3+; and R element between node 12b and S3-) having a nominal value of R to couple said first segment (10 - 12 [R 2R ladder]) and said second segment (13 [2R 2R]).

Regarding claim 19, wherein the first (10a – 12a [R 2R ladder]) and second (10b – 12b [R 2R ladder]) ladders comprise R2R ladders and said second segment (13b [2R 2R]) comprises a 2R pair array, and wherein resistors of the first ladder are cross mixed with the second ladder resistors (Fig. 5 disclosing first [10a – 12a] and second [10b – 12b] R2R ladders are cross mixed through the switches) on an integrated circuit (Col. 1 lines 13 – 14).

Regarding claim 20, Fig. 7 further comprising a filter (R3, R2, C1, C2 filter circuit, See Col. 8 lines 4 – 23) coupled to the differential output (Vp, Vn), wherein said filter has a gain sufficient to not require a buffer between the differential output and the filter (Fig. 7 does not disclose any buffer located between the filter and the differential output Vp, Vn of R- 2R Digital to Analog converter 72, therefore the RC filter of Valdenaire must has sufficient gain).

Regarding claim 12, wherein said first segment is a least significant bit section (Fig. 5 of Valdenaire as applied to claim 11 above and on Col. 3 lines 5 - 9, disclosing first segment 10 – 12 [R 2R] having differential input [10a and 10b] is a most significant bit section and second segment 13 [2R 2R] couple to the first segment having differential output [15 Vp, 14 Vn] is a least significant bit section). Furthermore, on Col.7 lines 32 – 34, Valdernaire teaches the node [14, 15] is a reference input, and the differential input [10a, 10b] is an output node. Hence 14 and 15 become the input nodes, and 10a and 10b become the output nodes in Fig. 5., the segment (13 [2R 2R]) now having differential input (14, 15), the segment (10 – 12 [R 2R]) now having differential output [10a 10b], wherein the segment (13 [2R 2R]) is a least significant bit

section and the segment (10 – 12[R 2R]) is a most significant bit section (Col. 3 lines 5 – 9).

Regarding claim 13, wherein said second segment is a most significant bit section (Fig. 5 of Valdenaire as applied to claim 11 above and on Col. 3 lines 5 - 9, disclosing first segment 10 – 12 [R 2R] having differential input [10a and 10b] is a most significant bit section, and second segment 13 [2R 2R] couple to the first segment having differential output [15 Vp, 14 Vn] is a least significant bit section). Furthermore, on Col.7 lines 32 – 34, Valdenaire further teaches the node [14, 15] is a reference input, and the input [10a, 10b] is an output node. Hence 14 and 15 become the input nodes, and 10a and 10b become the output nodes in Fig. 5., the segment (13 [2R 2R]) now having differential input (14, 15), the segment (10 – 12 [R 2R]) now having differential output [10a 10b], wherein the segment (13 [2R 2R]) is a least significant bit section and the segment (10 – 12[R 2R]) is a most significant bit section (Col. 3 lines 5 – 9).

However, Valdenaire as applied to claims 11 – 15, and 17 – 20 above, does not disclose that its converter is used in a transceiver; and an omnidirectional antenna coupled to the transceiver.

Fig. 1 of Dogan discloses a transceiver; an omnidirectional antenna (Col. 4 lines 38 – 39) coupled to the transceiver, and the transceiver is using a digital-to-analog converter (237, See Col. 4 lines 24 – 27).

It is obvious to use the digital-to-analog converter of Valdenaire in an environment where a transceiver is needed or a general combination of system elements to provide a particular end result. One a particular end result is known from

the viewpoint of overall system, it would be obvious to use a particular circuit with specifics components as discussed in Dogan to meet refinement for that specific use. This refinement of know circuitry such as that taught in Dogan is well known in the design and use of circuitry in the production and manufacturing of an electronic system and is considered to be routine part of the final stages prior to final preparation for sale and end use.

Allowable Subject Matter

7. Claims 6 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, the prior art does not teach wherein the first ladder is coupled to a current sourcing input buffer, and wherein the second ladder is coupled to a current sinking buffer.

Cited References

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited references relate of Digital to Analog converter in a communication system.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (571)

272-1810. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Michael Tokar can be reached at (571) 272-1812. The fax phone numbers for the organization where this application or proceeding is assigned are (703-872-9306) for regular communications and (703-872-9306) for After Final communications.

09/30/2004

Linh Van Nguyen 

Art Unit 2819